

ESD PROTECTION DEVICE HAVING REDUCED TRIGGER VOLTAGE

Abstract

An electrostatic discharge (ESD) protection device having reduced trigger voltage is disclosed. A substrate of first conductivity type is provided. A first MOS transistor of second conductivity type is disposed on the substrate. The first MOS transistor comprises a first gate, a first gate dielectric disposed under the first gate, a first heavily doped region of the second conductivity type implanted into the substrate at one side of the first gate, and a second heavily doped region of the second conductivity type implanted into the substrate at the other side of the first gate. A second MOS transistor of the second conductivity type is laterally disposed on the substrate in proximity to the first MOS transistor. The second MOS transistor comprises a second gate, a second gate dielectric disposed under the second gate, a third heavily doped region of the second conductivity type implanted into the substrate at one side of the second gate, and a fourth heavily doped region of the second conductivity type implanted into the substrate at the other side of the second gate. At least one float-

ing gate MOS transistor comprising a floating gate dielectric is formed on the substrate. A floating gate overlies the floating gate dielectric. The floating gate MOS transistor is located between the first MOS transistor and the second MOS transistor. The floating gate MOS transistor is serially connected to the first MOS transistor via the second heavily doped region and is serially connected to the second MOS transistor via the third heavily doped region.